IN THE CLAIMS

1. (Previously Presented) An integrated circuit, comprising:

a plurality of switches;

a first conductor having a first span along a first dimension, the first conductor to selectively couple to at least one input of each of at least two adjacent program controlled cells through a respective first switch and second switch of the plurality of switches without requiring traversal of another conductor;

a second conductor having a second span along the first dimension;

a third conductor having a third span along the first dimension, the third span being different than the second span, the first conductor to selectively couple to the second conductor and the third conductor;

a fourth conductor having a fourth span along a second dimension; and

a fifth conductor having a fifth span along the second dimension, the fourth span being different than the fifth span, and each of the fourth conductor and the fifth conductor selectively coupled to drive the first conductor through a respective independently controlled third switch and fourth switch of the plurality of switches, and wherein each of the first, second, third, fourth and fifth conductors is neither an input nor an output of a program controlled cell.

2. (Original) The integrated circuit of claim 1, wherein each of the plurality of switches comprises at least a program controlled passgate.

3. (Original) The integrated circuit of claim 1, wherein each of the plurality of switches comprises at least a program controlled driver/receiver.

4. (Previously Presented) The integrated circuit of claim 1, wherein one of the plurality of switches comprises at least one of a program controlled passgate and a program controlled driver/receiver.

5. (Original) The integrated circuit of claim 1, wherein one of the plurality of switches has a program controlled on state and off state.

6. (Original) The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating memory devices.

7. (Original) The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

8. (Original) The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

9. (Original) The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

10. (Original) The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating Ferro-electric devices.

11. (Previously Presented) A method, comprising:

providing a plurality of switches;

providing a first conductor having a first span along a first dimension;

selectively coupling the first conductor to at least one input of each of at least two adjacent program controlled cells through a respective first switch and second switch of the plurality of switches without requiring traversal of another conductor;

providing a second conductor having a second span along the first dimension; and

providing a third conductor having a third span along the first dimension, the third span being different than the second span;

selectively coupling the first conductor to the second conductor and the third conductor;

providing a fourth conductor having a fourth span along a second dimension; and

providing a fifth conductor having a fifth span along the second dimension, the fifth span being different than the fourth span; and

driving the first conductor using each of the fourth and the fifth conductors through a respective independently controlled third switch and fourth switch of the plurality of switches.

12. (Original) The method of claim 11, wherein each of the plurality of switches comprises at least a program controlled driver/receiver.

13. (Previously Presented) The method of claim 11, wherein one of the plurality of switches comprises at least one of a program controlled passgate and a program controlled driver/receiver.

14. (Original) The method of claim 11, wherein one of the plurality of switches has a program controlled on state and off state.

15. (Original) The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating memory devices.

16. (Original) The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

17. (Original) The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

18. (Original) The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

19. (Original) The method of claim 11, wherein the integrated circuit is implemented using process technology incorporating Ferro-electric devices.

20. (Previously Presented) An integrated circuit having a span comprising:

a first conductor and a second conductor, each having a respectively different first span and second span along a first dimension, each of the first conductor and the second conductor being neither an input nor an output of a program controlled cell, wherein the second span is greater than the first span, and wherein the second span is less than the span of the integrated circuit along the first dimension and the first span and the second span are spanning at least one common program controlled cell along the first dimension;

a third conductor and a fourth conductor , each having a respectively different third span and fourth span along a second dimension, each of the third conductor and the fourth conductor being neither an input nor an output of a program controlled cell, wherein the fourth span is greater than the third span, wherein the third span is no less than the first span, and wherein the fourth span is less than the span of the integrated circuit along the second dimension , and wherein the third span and the fourth span are spanning at least one common program controlled cell along the second dimension; and

a first switch and a second switch, the first conductor to selectively couple to the third conductor through the first switch without requiring traversal of another conductor, and the first conductor to selectively couple to the fourth conductor through the second switch without requiring traversal of another conductor.

21. (Previously Presented) The integrated circuit as set forth in claim 20, further comprising a third switch, and wherein the second conductor is configured to selectively couple to the fourth conductor through the third switch without requiring traversal of another conductor.

22. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit consists of a core.

23. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit consists of a core and I/O to core interfaces.

24. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit excludes I/O logic blocks.

25. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit excludes I/O logic blocks and I/O to core interfaces.

26. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the switches comprise program controlled passgates.

27. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the switches comprise program controlled drivers/receivers.

28. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the switches comprise program controlled passgates and program controlled drivers/receivers.

29. (Previously Presented) The integrated circuit as set forth in claim 20, wherein at least one of the switches has a program controlled on state and off state.

30. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit is implemented using process technology incorporating memory devices.

31. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

32. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

33. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

34. (Previously Presented) The integrated circuit as set forth in claim 20, wherein the integrated circuit is implemented using process technology incorporating ferro-electric devices.

35. (Previously Presented) A method comprising:

providing a first conductor and a second conductor, each having a respectively different first span and second span along a first dimension, each of the first conductor and the second conductor being neither an input nor an output of a program controlled cell, wherein the second span is greater than the first span, wherein the second span is less than a span of the integrated circuit along the first dimension, and wherein the first span and the second span are spanning at least one common program controlled cell along the first dimension;

providing a third conductor and a fourth conductor , each having a respectively different third span and fourth span along a second dimension, each of the third conductor and the fourth conductor being neither an input nor an output of a program controlled cell, wherein the fourth span is greater than the third span, wherein the third span is no less than the first span, wherein the fourth span is less than the span of the integrated circuit along the second dimension, and wherein the third span and the fourth span are spanning at least one common program controlled cell along the second dimension; and

providing a first switch and a second switch, the first conductor to selectively couple to the third conductor through the first switch without requiring traversal of another conductor, and the first conductor to selectively couple to the fourth conductor through the second switch without requiring traversal of another conductor.

36. (Previously Presented) The method as set forth in claim 35, further comprising selectively coupling the second conductor to the fourth conductor through the third switch without requiring traversal of another conductor.

37. (Previously Presented) The method as set forth in claim 35, wherein the integrated circuit consists of a core.

38. (Previously Presented) The method as set forth in claim 35, wherein the integrated circuit consists of a core and I/O to core interfaces.

39. (Previously Presented) The method as set forth in claim 35, wherein the integrated circuit excludes I/O logic blocks.

40. (Previously Presented) The method as set forth in claim 35, wherein the integrated circuit excludes I/O logic blocks and I/O to core interfaces.

41. (New) The integrated circuit as set forth in claim 25, wherein at least one of the first switch and the second switch consists of a single anti-fuse device.

42. (New) The method as set forth in claim 40, wherein at least one of the first switch and the second switch consists of a single anti-fuse device.